AMENDMENTS TO THE CLAIMS

Claims 1-44 (canceled).

45. (original) A photodiode sensor for use in an imaging device, said photodiode sensor comprising:

a doped layer of a first conductivity type formed in a substrate;

a plurality of trenches formed in said doped layer, each of said plurality of trenches having a plurality of sidewalls and a bottom, each of said plurality of trenches having a depth within the range of approximately 0.05 to 10 μm; and

a doped region of a second conductivity type formed at the sidewalls and bottom of each of said plurality of trenches.

46. (original) The photodiode sensor of claim 45, wherein the first conductivity type is p-type and the second conductivity type is n-type.

47. (original) The photodiode sensor of claim 45, wherein the doped region is formed by a process of multiple angled ion implantation.

48. (original) The photodiode sensor of claim 47, wherein the process comprises four orthogonal angled implants at a dose of 1×10^{12} to 1×10^{16} ions/cm^2, wherein a resist is placed on top of the substrate while implanting, and wherein the angle of implantation for each angled implant is greater than θ_C, where $\tan \theta_C = [(t + d)/(w)]$, where t is the thickness of the resist, d is the depth of said plurality of trenches, and w is the width of said plurality of trenches.

49. (original) The photodiode sensor of claim 48, wherein the dose of each implant is 1×10^{13} to 1×10^{15} ions/cm^2.

50. (original) The photodiode sensor of claim 48, wherein the dose of each implant is 5×10^{13} ions/cm^2.

51. (original) The photodiode sensor of claim 45, wherein said plurality of trenches comprises two trenches.

Claims 52-73 (canceled).

74. (original) A pixel sensor cell for use in an imaging device, said pixel sensor cell comprising:

a doped layer of a first conductivity type formed in a substrate;

a plurality of trenches formed in said doped layer, each of said plurality of trenches having a plurality of sidewalls and a bottom;

a photogate formed in each of said plurality of trenches, wherein said photogate comprises a first doped region of a second conductivity type formed at the sidewalls and bottom of each of said plurality of trenches, a conductive layer formed on substantially all of an upper surface of said first doped region for gating the collection of charges in said first doped region, and an insulating layer formed between said first doped region and said conductive layer;

a second doped region of a second conductivity type formed in said doped layer and positioned to receive charges from said first doped region of each of said plurality of trenches; and

a reset transistor formed at the doped layer for periodically resetting a charge level of said second doped region, said second doped region being the source of said reset transistor.

75. (Original) A pixel sensor cell for use in an imaging device, said pixel sensor cell comprising:

a plurality of trench photosensors formed in a doped layer of a first conductivity type of a substrate;

a reset transistor formed in said doped layer; and

a floating diffusion region of a second conductivity type formed in said doped layer between said plurality of trench photosensors and the reset transistor for receiving charges from said plurality of trench photosensors, said reset transistor operating to periodically reset a charge level of said floating diffusion region; and

an output transistor having a gate electrically connected to the floating diffusion region.

76. (original) The pixel sensor cell of claim 75, wherein each of said plurality of trench photosensors further comprises a doped region of a second conductivity type located on the sidewalls and bottom of each of said plurality of trenches.

77. (original) The pixel sensor cell of claim 75, wherein each of said plurality of trench photosensors is a photodiode sensor.

78. (original) The pixel sensor cell of claim 75, further comprising a transfer gate located between the plurality of trench photosensors and the floating diffusion region.

79. (original) The pixel sensor cell of claim 78, wherein each of said plurality of trench photosensors is a photogate sensor.

80. (original) The pixel sensor cell of claim 75, wherein the first conductivity type is p-type, and the second conductivity type is n-type.

81. (original) The pixel sensor cell of claim 75, wherein said plurality of trench photosensors comprises two trench photosensors.

82. (original) A CMOS imager comprising:

a substrate having a doped layer of a first conductivity type;

an array of pixel sensor cells formed in said doped layer, wherein each pixel sensor cell has a plurality of trench photosensors; and

signal processing circuitry electrically connected to receive and process output signals from said array.

83. (original) The CMOS imager of claim 82, wherein each of said plurality of trench photosensors further comprises a doped region of a second conductivity type located on the sidewalls and bottom of each of said plurality of trenches.

84. (original) The CMOS imager of claim 83, wherein the second conductivity type is n-type.

85. (original) The CMOS imager of claim 82, wherein each of said plurality of trench photosensors is a photodiode sensor.

86. (original) The CMOS imager of claim 82, wherein each of said plurality of trench photosensors is a photogate sensor.

87. (original) The CMOS imager of claim 82, wherein the first conductivity type is p-type.

88. (original) An integrated circuit imager comprising:

an array of pixel sensor cells formed in a substrate, wherein each pixel sensor cell has a plurality of trench photosensors;

signal processing circuitry formed in said substrate and electrically connected to the array for receiving and processing signals representing an image output by the array and for providing output data representing said image; and

a processor for receiving and processing data representing said image.

89. (original) An integrated circuit imager comprising:

a CMOS imager, said CMOS imager comprising an array of pixel sensor cells formed in a doped layer on a substrate, wherein each pixel sensor cell has a plurality of trench photosensors with a first doped region formed therein, each of said cells having a respective second doped region for receiving and outputting image charge received from said first doped region, and signal processing circuitry formed in said substrate and electrically connected to the array for receiving and processing signals representing an image output by the array and for providing output data representing said image; and

a processor for receiving and processing data representing said image.

Claims 90-116 (canceled).